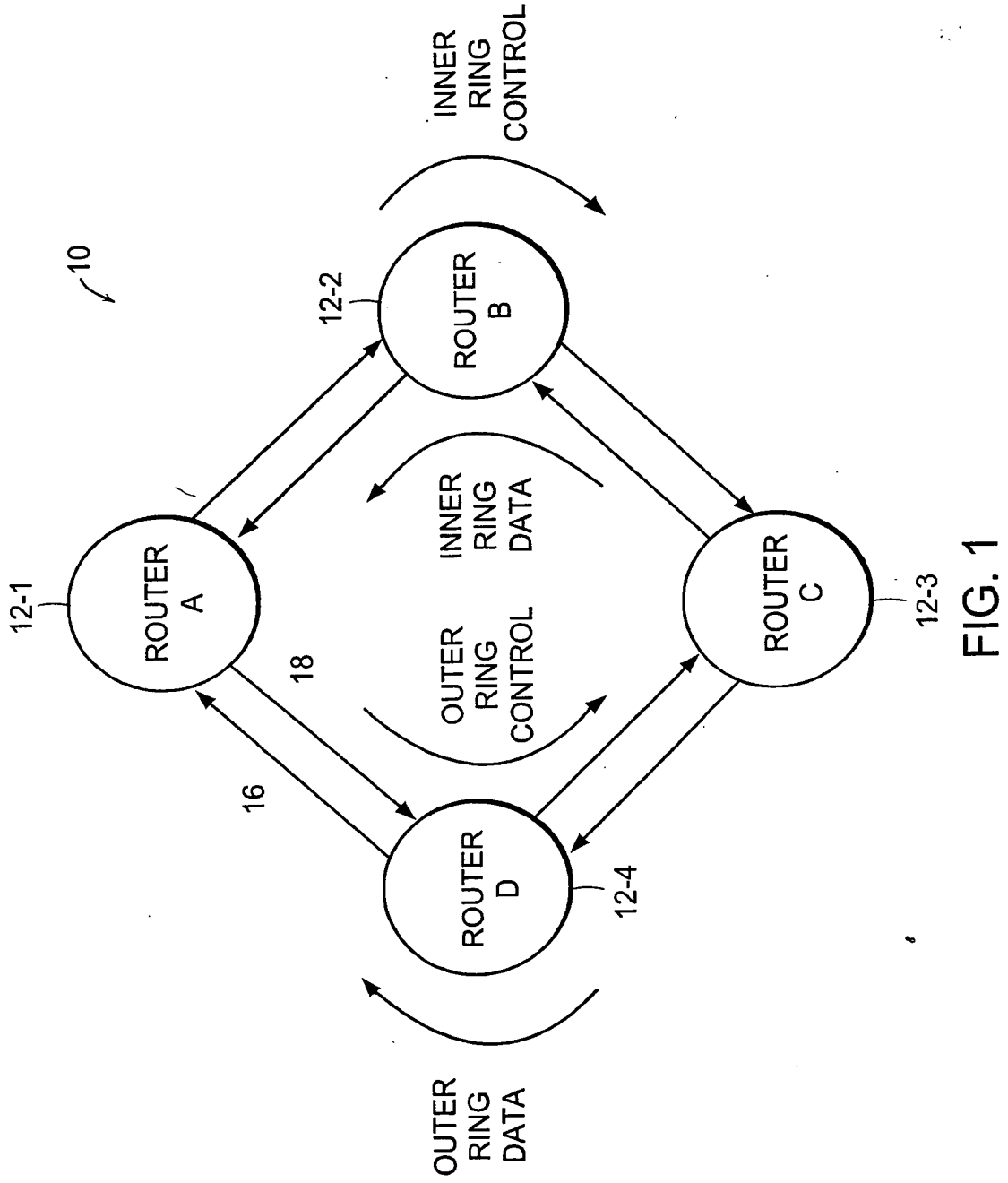

10
ROUTER A
12-1
ROUTER B
12-2
ROUTER C
12-3
ROUTER D
12-4
16
18
INNER RING CONTROL
INNER RING DATA
OUTER RING CONTROL
OUTER RING DATA

FIG. 1

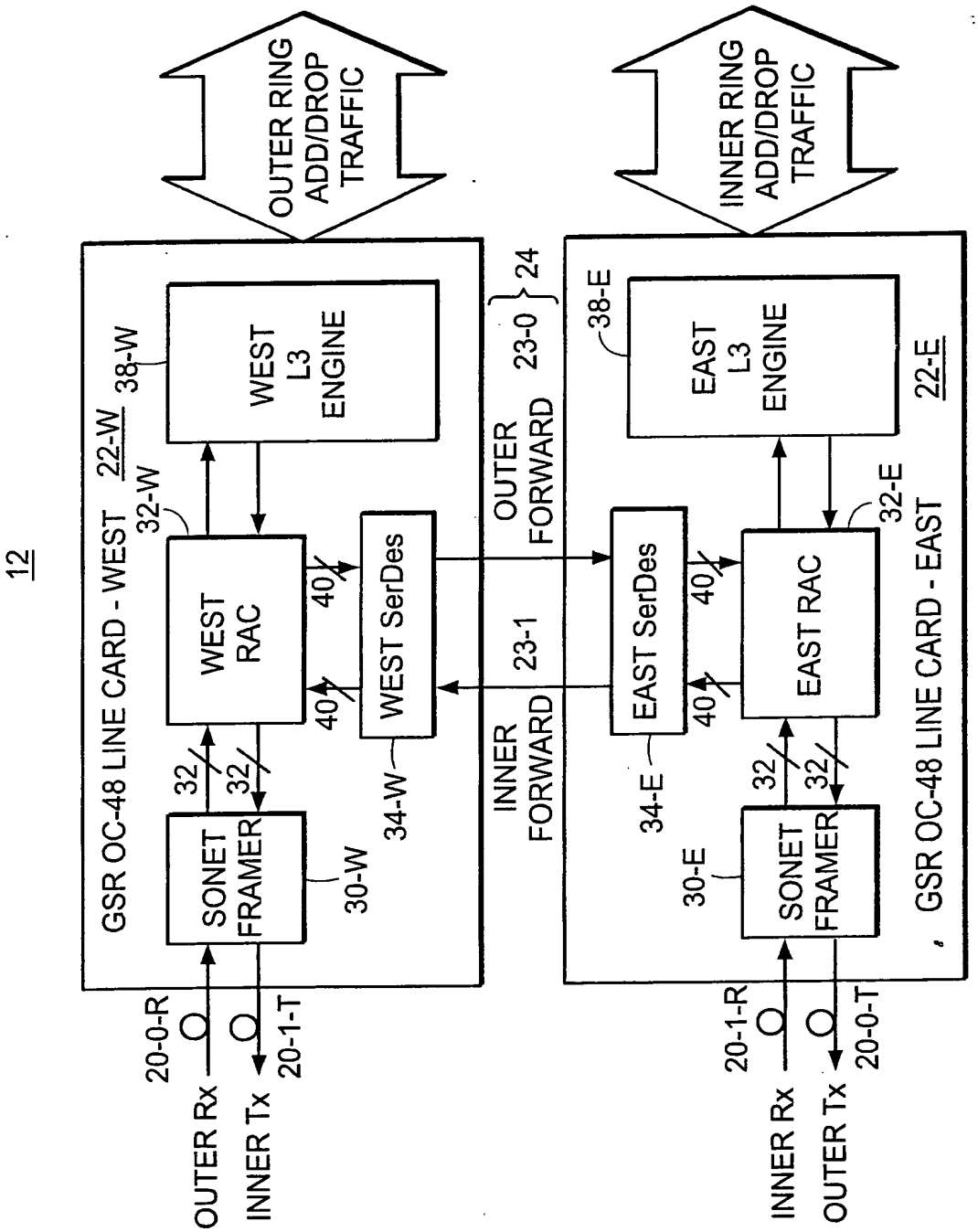

12
OUTER RING ADD/DROP TRAFFIC
INNER RING ADD/DROP TRAFFIC
GSR OC-48 LINE CARD - WEST
22-W
38-W
WEST L3 ENGINE
32-W
WEST RAC
40
40
WEST SerDes
34-W
32
32
SONET FRAMER
30-W
20-0-R
20-1-T
OUTER Rx
INNER Tx
OUTER FORWARD
23-0
24
INNER FORWARD
23-1
GSR OC-48 LINE CARD - EAST
22-E
38-E
EAST L3 ENGINE
32-E
EAST RAC
40
40
EAST SerDes
34-E
32
32
SONET FRAMER
30-E
20-1-R
20-0-T
INNER Rx
OUTER Tx

FIG. 2

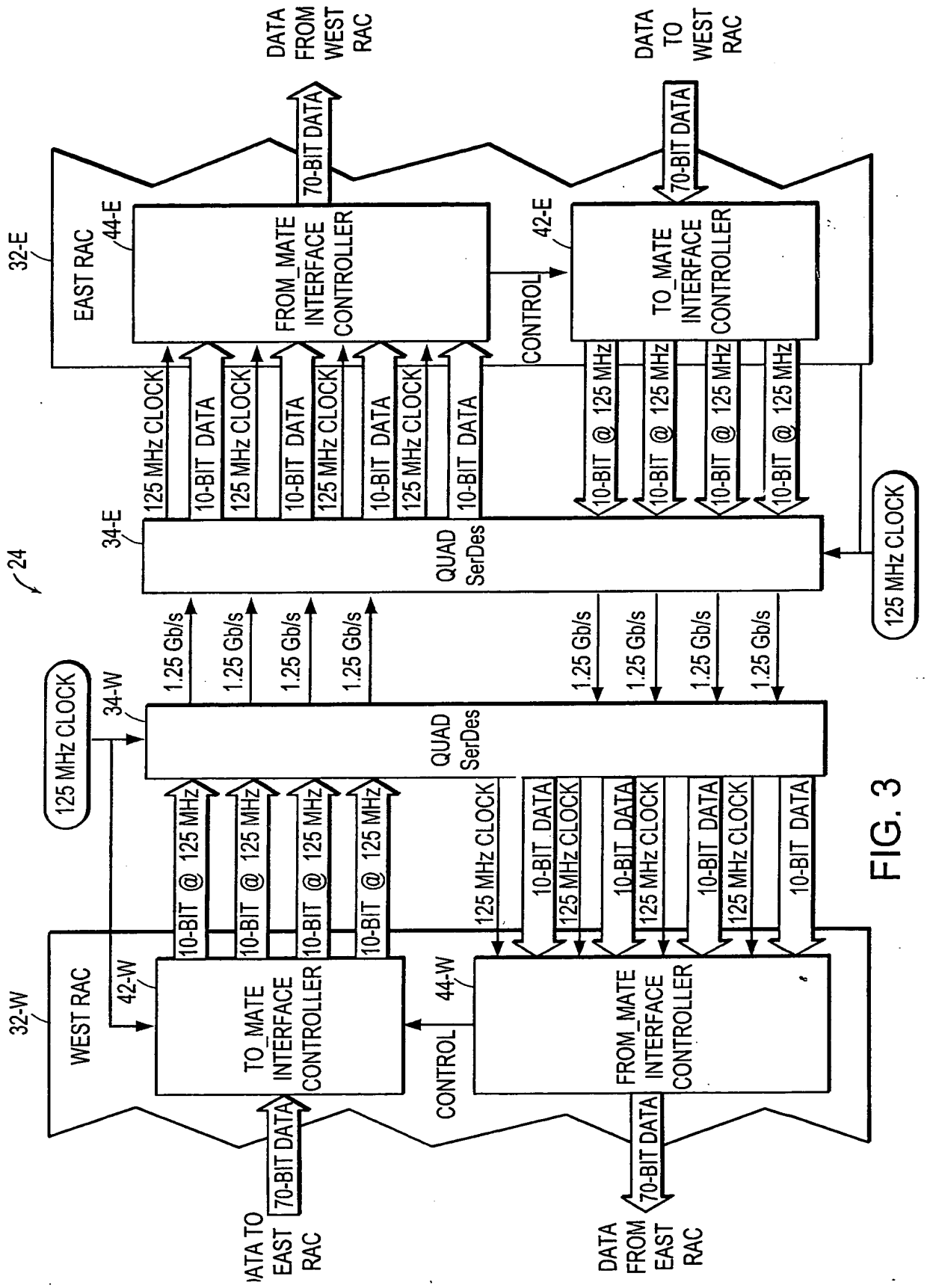

DATA FROM WEST RAC
DATA TO WEST RAC
70-BIT DATA
70-BIT DATA
32-E
EAST RAC
44-E
FROM_MATE INTERFACE CONTROLLER
42-E
TO_MATE INTERFACE CONTROLLER
CONTROL
125 MHz CLOCK
10-BIT DATA
10-BIT @ 125 MHz
34-E
QUAD SerDes
24
1.25 Gb/s
125 MHz CLOCK
34-W
QUAD SerDes
125 MHz CLOCK
32-W
WEST RAC
42-W
TO_MATE INTERFACE CONTROLLER
44-W
FROM_MATE INTERFACE CONTROLLER
CONTROL
70-BIT DATA
DATA TO EAST RAC
DATA FROM EAST RAC

FIG. 3

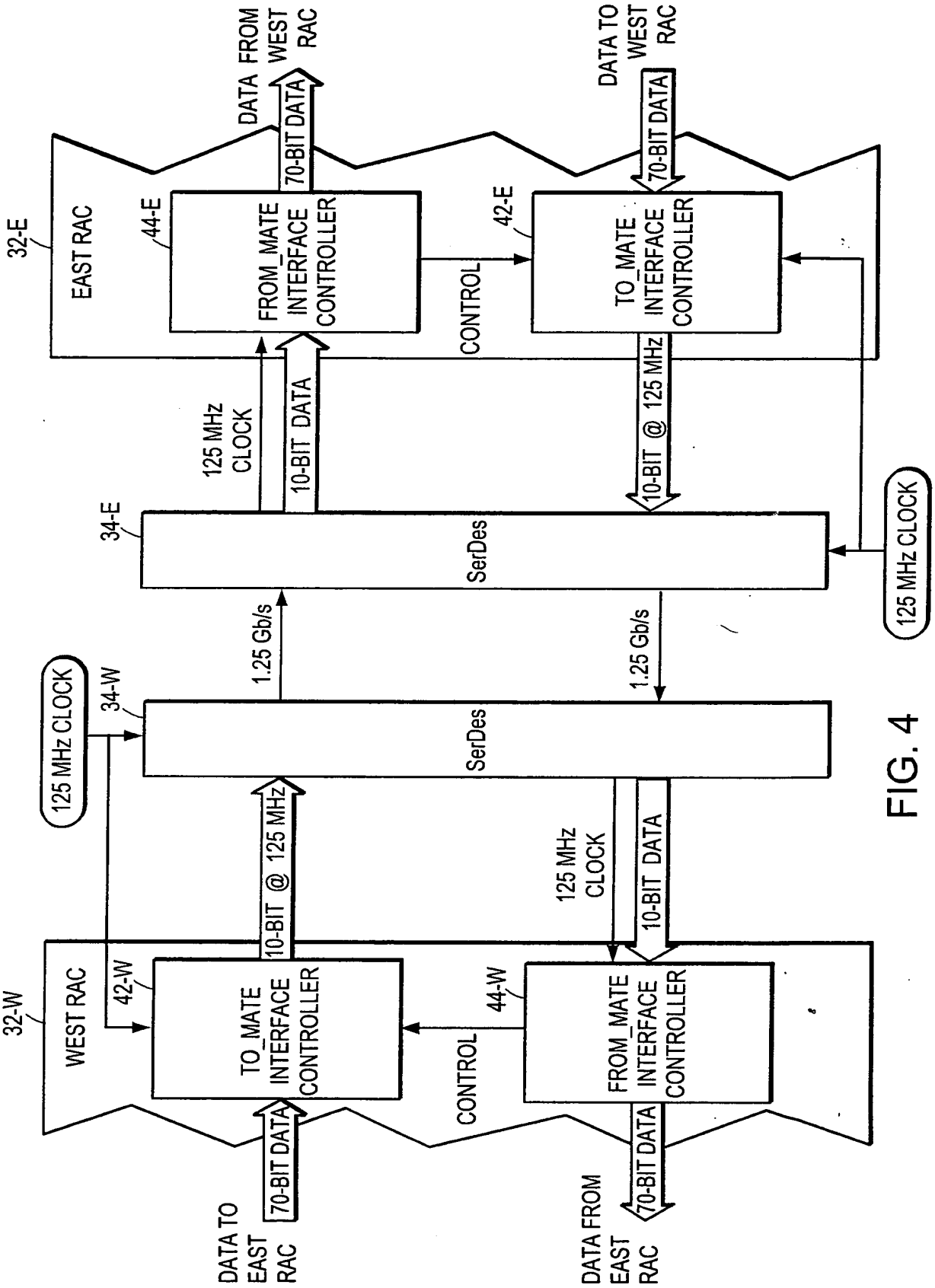

DATA FROM WEST RAC
70-BIT DATA
DATA TO WEST RAC
70-BIT DATA
32-E
EAST RAC
44-E
FROM_MATE INTERFACE CONTROLLER
CONTROL
42-E
TO_MATE INTERFACE CONTROLLER
125 MHz CLOCK
10-BIT DATA
10-BIT @ 125 MHz
34-E
SerDes
125 MHz CLOCK
1.25 Gb/s
1.25 Gb/s
125 MHz CLOCK
34-W
SerDes
10-BIT @ 125 MHz
125 MHz CLOCK
10-BIT DATA
32-W
WEST RAC
42-W
TO_MATE INTERFACE CONTROLLER
CONTROL
44-W
FROM_MATE INTERFACE CONTROLLER
70-BIT DATA
70-BIT DATA
DATA TO EAST RAC
DATA FROM EAST RAC

FIG. 4

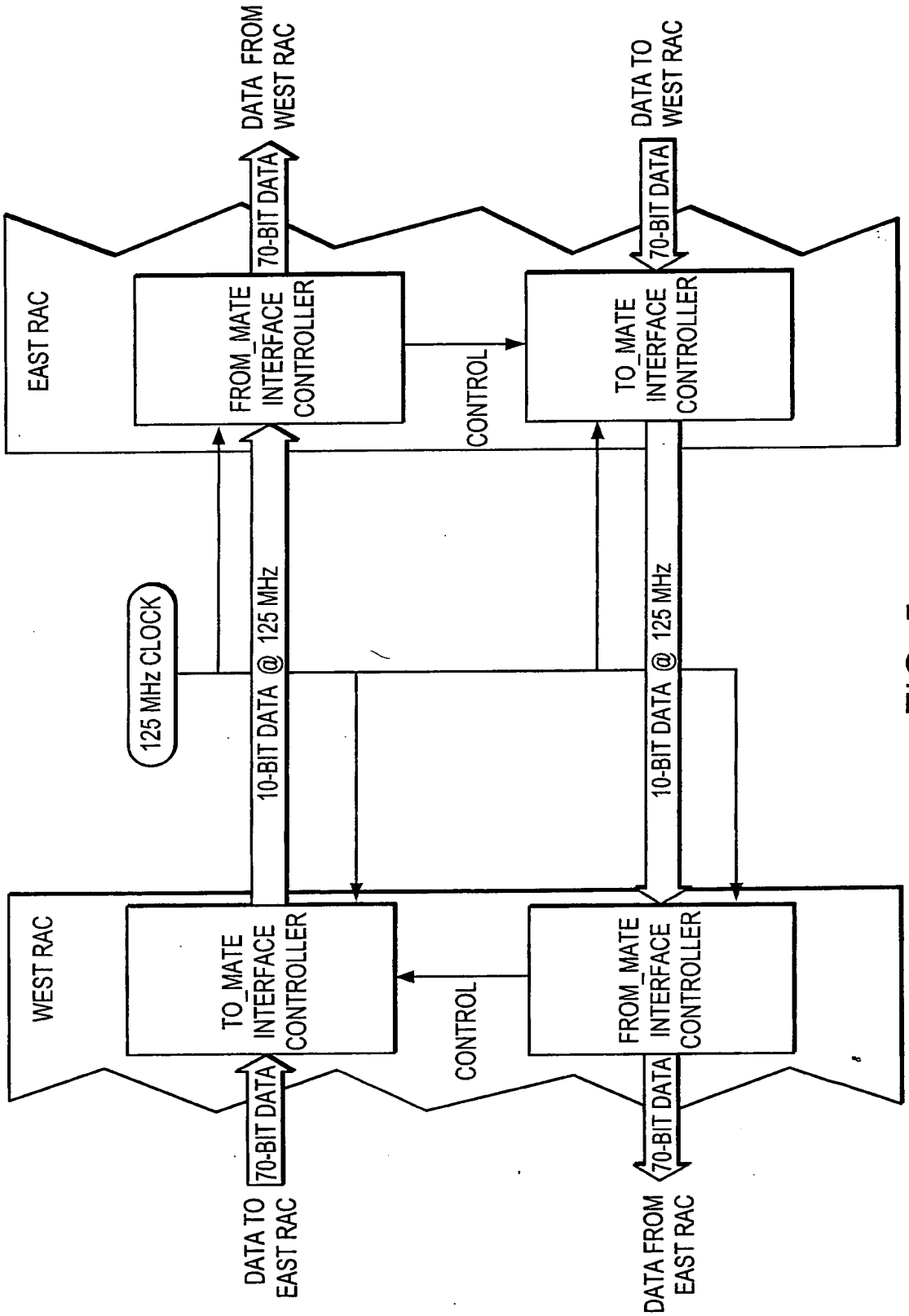

DATA FROM WEST RAC
70-BIT DATA
DATA TO WEST RAC
70-BIT DATA
EAST RAC
FROM_MATE INTERFACE CONTROLLER
CONTROL
TO_MATE INTERFACE CONTROLLER
125 MHz CLOCK
10-BIT DATA @ 125 MHz
10-BIT DATA @ 125 MHz
WEST RAC
TO_MATE INTERFACE CONTROLLER
CONTROL
FROM_MATE INTERFACE CONTROLLER
70-BIT DATA
70-BIT DATA
DATA TO EAST RAC
DATA FROM EAST RAC

FIG. 5

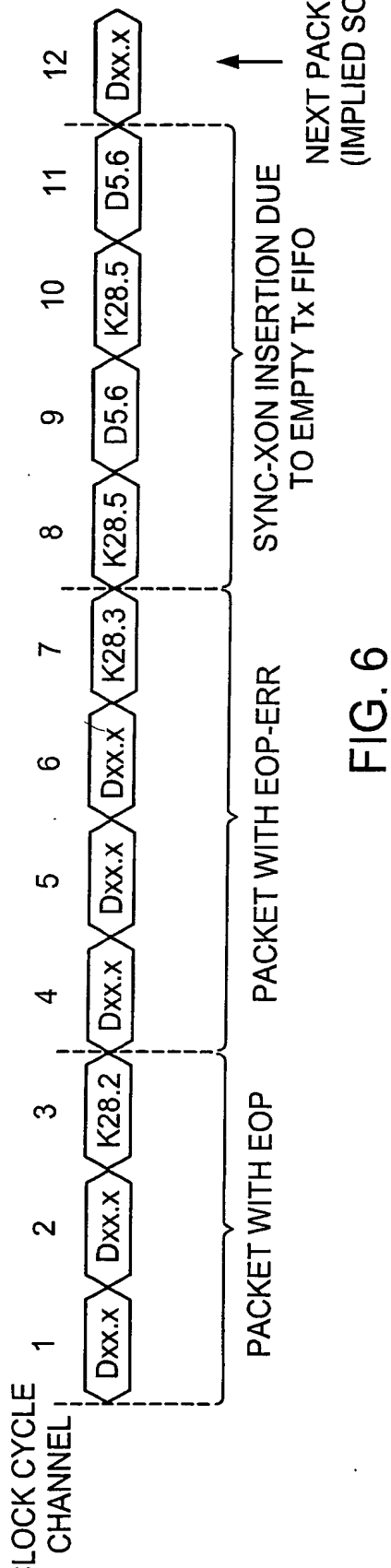

:LOCK CYCLE
CHANNEL
1
2
3
4
5
6
7
8
9
10
11
12
Dxx.x
Dxx.x
K28.2
Dxx.x
Dxx.x
Dxx.x
K28.3
K28.5
D5.6
D5.6
Dxx.x
PACKET WITH EOP
PACKET WITH EOP-ERR
SYNC-XON INSERTION DUE TO EMPTY Tx FIFO
NEXT PACKET (IMPLIED SOP)

FIG. 6

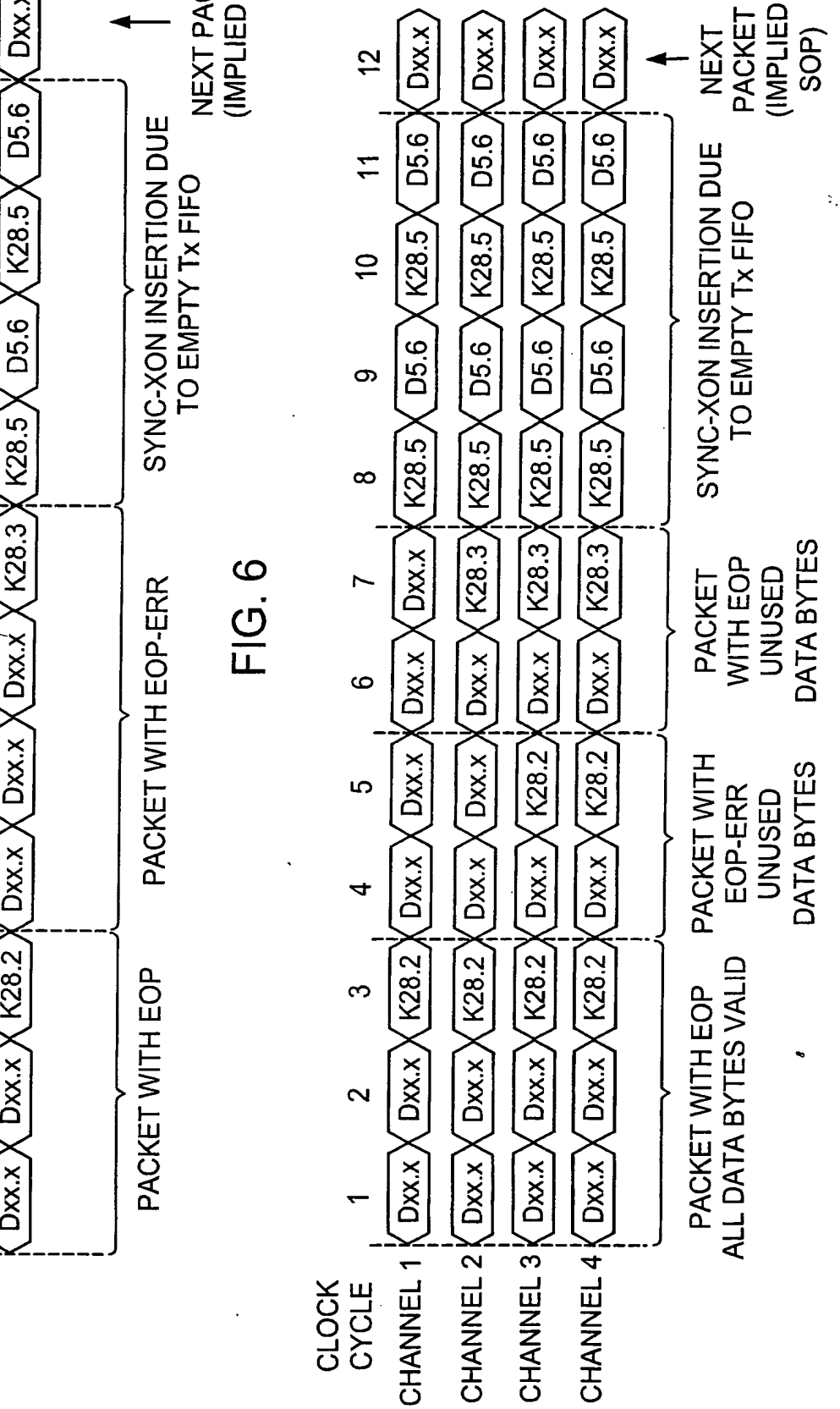

CLOCK CYCLE
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
1
2
3
4
5
6
7
8
9
10
11
12
Dxx.x
Dxx.x
K28.2
Dxx.x
Dxx.x
Dxx.x
K28.3
K28.5
D5.6
D5.6
Dxx.x
K28.2
K28.3
PACKET WITH EOP ALL DATA BYTES VALID
PACKET WITH EOP-ERR UNUSED DATA BYTES
PACKET WITH UNUSED DATA BYTES
SYNC-XON INSERTION DUE TO EMPTY Tx FIFO
NEXT PACKET (IMPLIED SOP)

FIG. 7

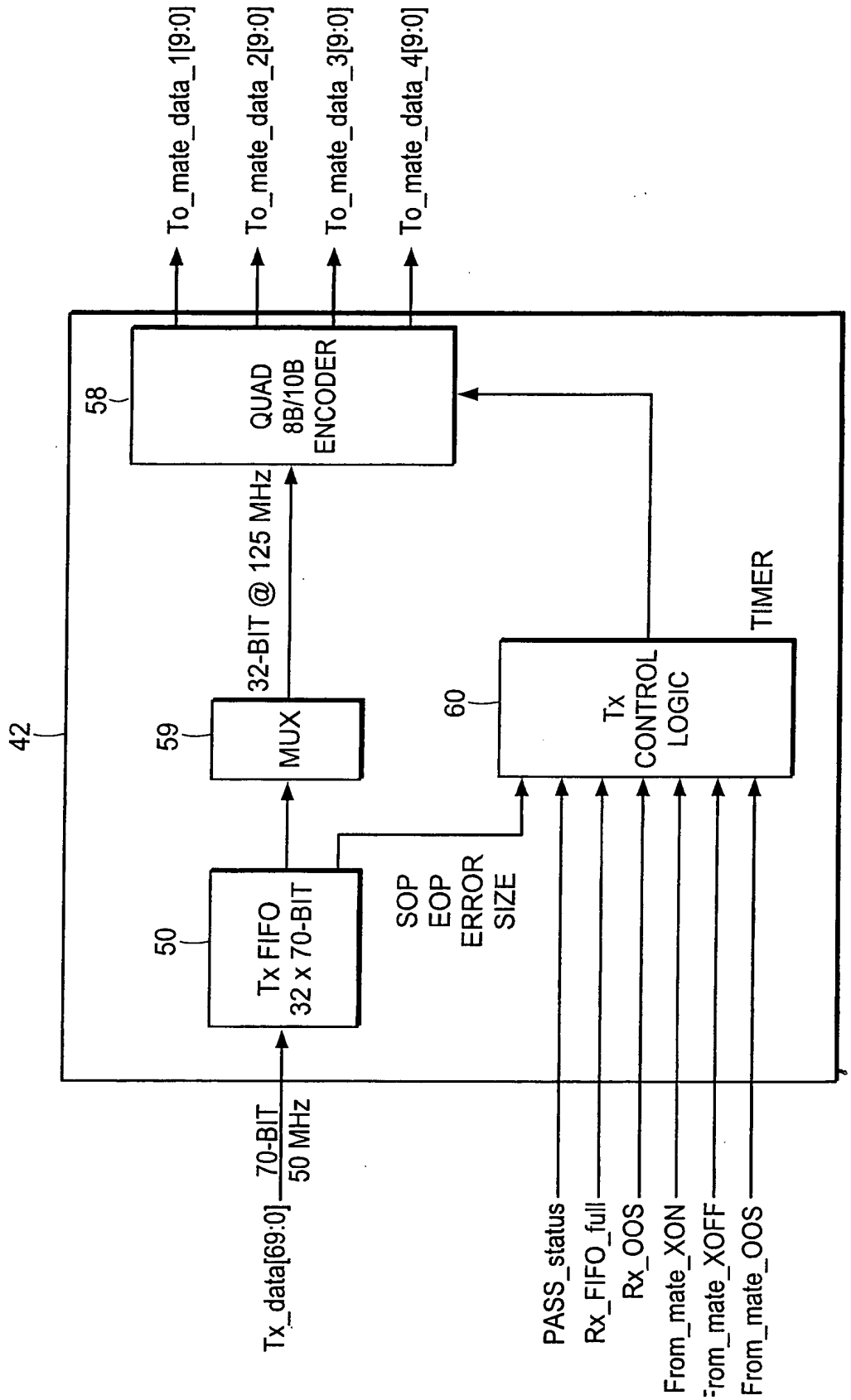
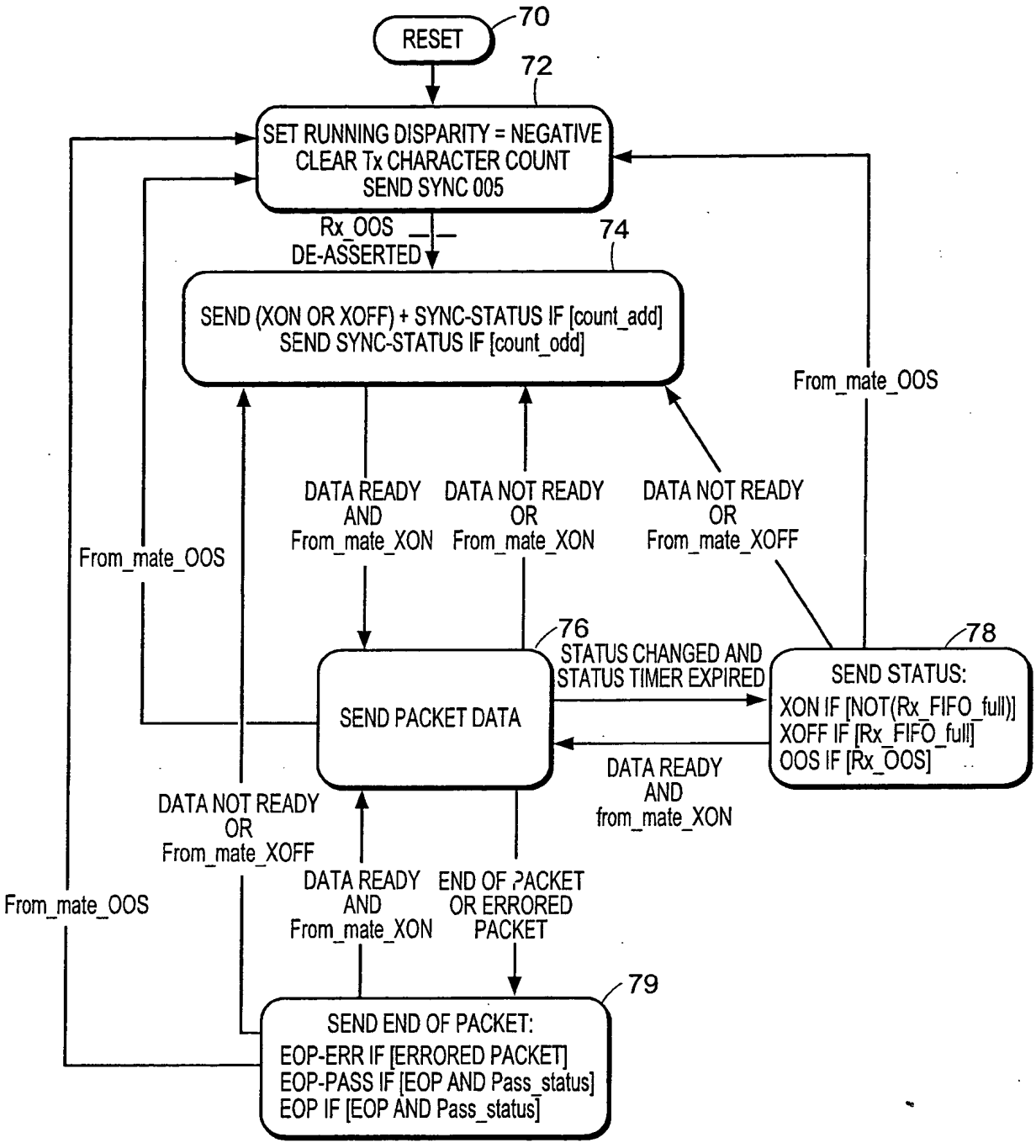

To_mate_data_1[9:0]
To_mate_data_2[9:0]
To_mate_data_3[9:0]
To_mate_data_4[9:0]
58
QUAD 8B/10B ENCODER
32-BIT @ 125 MHz
59
MUX
60
Tx CONTROL LOGIC
TIMER
42
50
Tx FIFO 32 x 70-BIT
SOP
EOP
ERROR
SIZE
Tx_data[69:0]
70-BIT
50 MHz
PASS_status
Rx_FIFO_full
Rx_OOS
From_mate_XON
From_mate_XOFF
From_mate_OOS

FIG. 8



DEFINITION OF SYNC STATUS:

SYNC-XON IF [NOT (Rx_FIFO_full) AND NOT (PASS_status)]
SYNC-XON-PASS IF [NOT (Rx_FIFO_full) AND PASS_status]
SYNC-XOFF IF [Rx_FIFO_full AND NOT (PASS_status)]
SYNC-XOFF-PASS IF [Rx_FIFO_full AND PASS_status]
SYNC-OOS IF [Rx_OOS]

FIG. 9

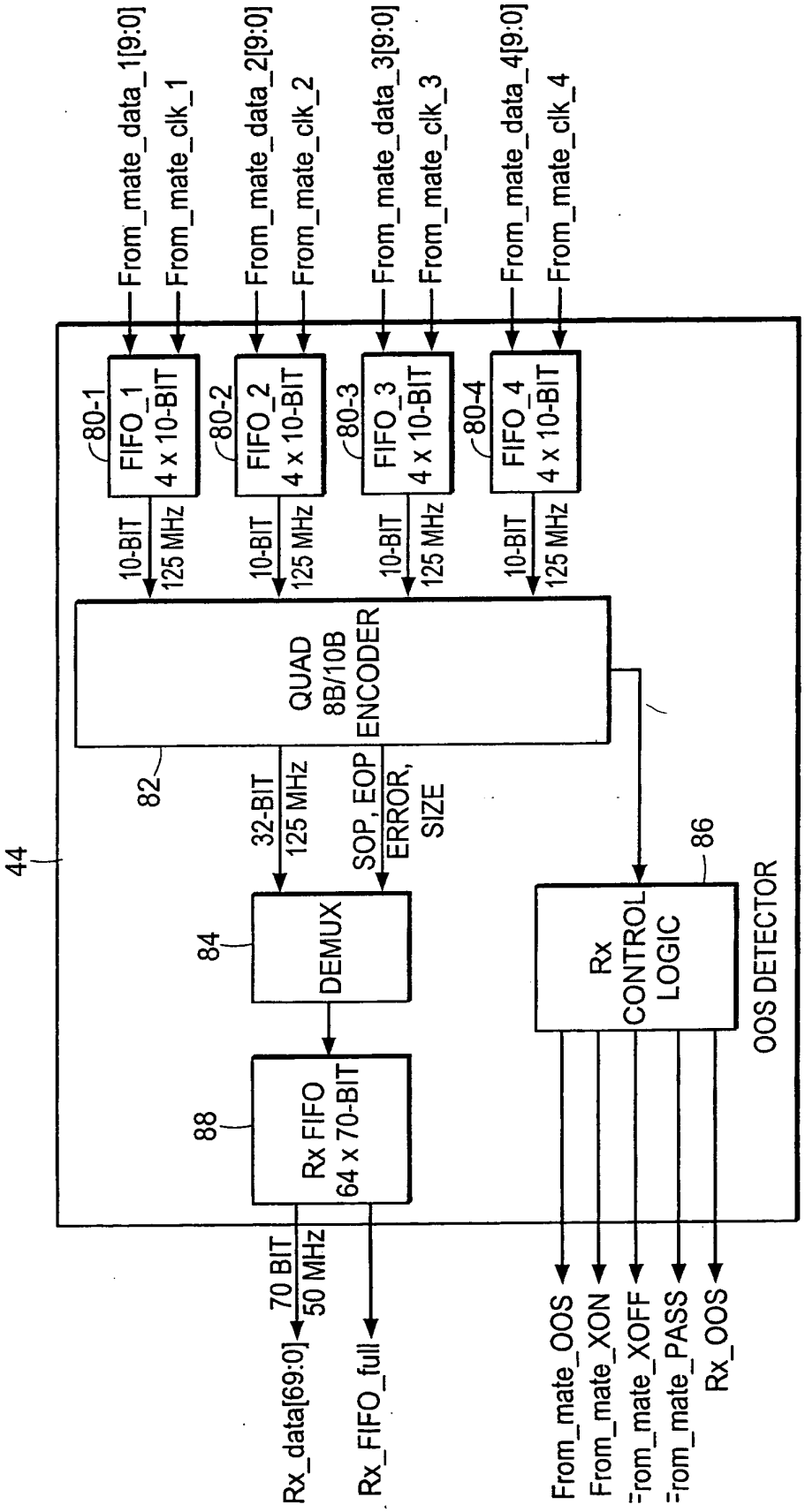

From_mate_data_1[9:0]
From_mate_clk_1
From_mate_data_2[9:0]
From_mate_clk_2
From_mate_data_3[9:0]
From_mate_clk_3
From_mate_data_4[9:0]
From_mate_clk_4
80-1
FIFO_1
4 x 10-BIT
80-2
FIFO_2
4 x 10-BIT
80-3
FIFO_3
4 x 10-BIT
80-4
FIFO_4
4 x 10-BIT
10-BIT
125 MHz
QUAD
8B/10B
ENCODER
82
32-BIT
125 MHz
SOP, EOP
ERROR,
SIZE
44
84
DEMUX
88
Rx FIFO
64 x 70-BIT
86
Rx
CONTROL
LOGIC
OOS DETECTOR
70 BIT
50 MHz
Rx_data[69:0]
Rx_FIFO_full
From_mate_OOS
From_mate_XON
From_mate_XOFF
From_mate_PASS
Rx_OOS

FIG. 10

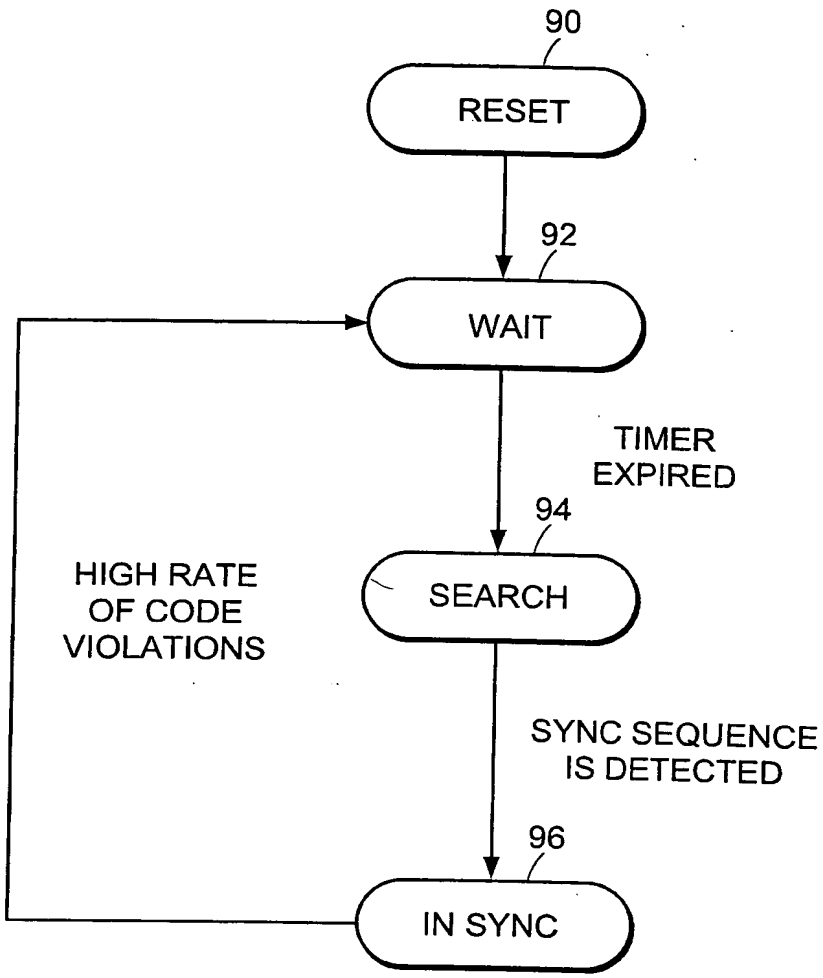

90
RESET
92
WAIT
TIMER
EXPIRED
94
SEARCH
HIGH RATE
OF CODE
VIOLATIONS
SYNC SEQUENCE
IS DETECTED
96
IN SYNC

FIG. 11

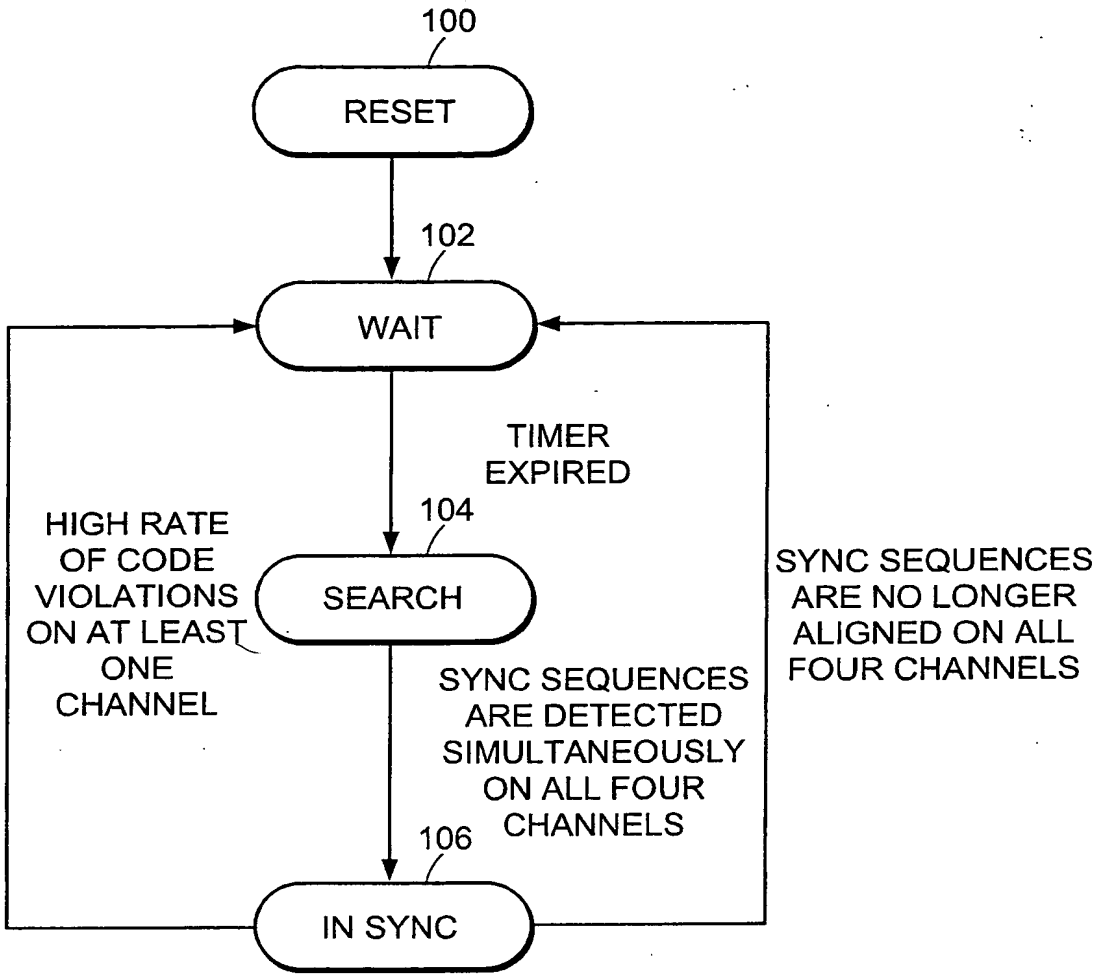

100
RESET
102
WAIT
TIMER EXPIRED
104
SEARCH
HIGH RATE OF CODE VIOLATIONS ON AT LEAST ONE CHANNEL
SYNC SEQUENCES ARE DETECTED SIMULTANEOUSLY ON ALL FOUR CHANNELS
106
IN SYNC
SYNC SEQUENCES ARE NO LONGER ALIGNED ON ALL FOUR CHANNELS

FIG. 12